

## CS61C: Circuits, CAD & Verilog

CS61C Fall2007 - Discussion #7  
Greg Gibeling

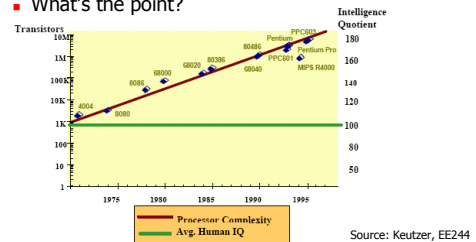
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## Quick Introduction to CAD (1)

- CAD = Computer Aided Design
- What's the point?



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## Quick Introduction to CAD (2)

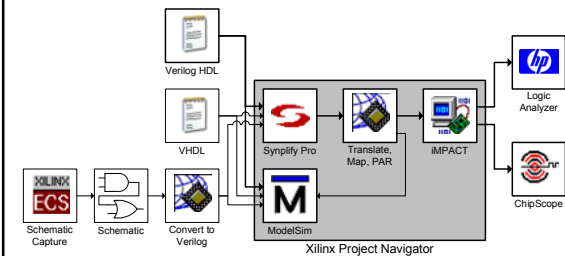
- CAD Tools
  - Special Editors
  - Data Processors
    - Synplify Pro
    - Xilinx Map & PAR Tools
    - ModelSim
- CAD Tool Flow
  - The tools and the order in which they are applied to a given design

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## Quick Introduction to CAD (3)

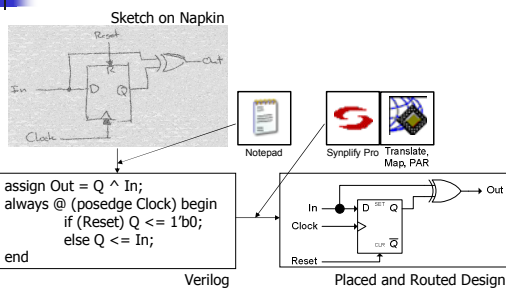


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## Quick Introduction to CAD (4)



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## Circuits Problems

- Design an Edge Detector
  - Takes a scalar signal in
  - Produces a single cycle pulse on change
- Combinational Feedback
  - Design a circuit which uses it properly
  - This is not an easy problem

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## Quick Introduction to CAD (5)

- Steps to build a circuit
  - Design the circuit (on paper)**
  - Write Verilog in Notepad
  - Simulate using ModelSim**
  - Fix the bugs
  - Re-simulate using ModelSim**
- In EECS150:
  - Synthesize
  - Program the Board

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## Verilog (1)





- What's an HDL?
  - Textual Description of a Circuit
  - Human and Machine Readable
  - Hierarchical
  - Meaningful Naming
- NOT A PROGRAM
  - Describe what the circuit IS
  - Not what it DOES

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## Verilog (2)

Digital Design Productivity, in Gates/Week

Source: DataQuest

Behavioral HDL		2K-10K
RTL HDL		1K-2K
Gates		100-200
Transistors		10-20

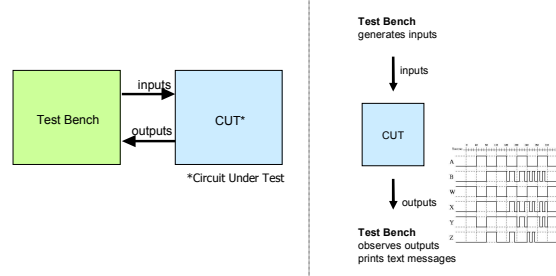
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## Testing & Verification (1)

- Develop a "Testbench"
  - A non-synthesized simple verilog module
  - Drive inputs
    - Random Test Vectors
    - Targeted Test Vectors <- Preferred
  - Check Outputs
- Coverage is Key!
  - How many potential problems were tested?

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## Testing & Verification (2)



Test Bench generates inputs

Test Bench observes outputs prints text messages

\*Circuit Under Test

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## Testing & Verification (3)

- ModelSim does "Functional Simulation"
  - Great for debugging!
  - Does not account for timing
    - Can be manually added in
- In EECS150
  - Xilinx PAR Tools Know More
    - After place and route, can extract timing
    - It is possible to feed timing into ModelSim
    - This produces a very accurate simulation
    - Great for checking reliability and efficiency

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## Testing & Verification (4)

- Hardware Verification
  - A long slow process
  - We prefer careful simulation earlier on
  - Bugs found here cost MILLIONS to fix
- We skip this
  - Does it LOOK like it works properly?
  - Close enough...

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## Using ModelSim

- Read the Tutorial
  - It'll be posted before Thursday
  - Read it ASAP
  - Ask questions ahead of time
  - Log in and run a basic example before lab if you want!

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